REMARKS

1. Objection to the disclosure because of an informality in paragraph [0026], "NLTPS 72" should be changed to "PLTPS 72":

Regarding the informality in paragraph [0026] of the specification, "NLTPS 72" has been revised to "PLTPS 72" to agree with the drawings. This amendment corrects a typographical error, and no new matter is introduced. Consideration of this amendment to the specification is requested.

2. Rejection of claims 1-2, 6-9, and 12-17 under 35 U.S.C. 103(a) as being unpatentable over the Admitted Prior Art (APA) in view of Ayres (US 6,632,709):

Claim 1 has been amended to recite the limitation of "performing a trimming process to remove a certain width of the first patterned photo resist layer". This limitation finds support in the specification in paragraph [0025] and Fig.8 for instance, and no new matter is entered.

Regarding to APA, the APA teaches a method of forming an N type LTPS TFT 34 and a P type LTPS TFT 36 comprising the steps of:

providing a substrate 10 comprising a first region I and a second region II (as shown in Fig.1);

sequentially forming a patterned undoped polysilicon layer 12, a dielectric layer 14, and a patterned conductive layer (gate electrode) 16, the patterned conductive layer 16 comprising two first gaps on both sides of the conductive layer 16 in the first region I (as shown in Fig.1);

performing a first implantation process to implant N type dopants 18 via the first gaps into the patterned undoped polysilicon layer 12 to form N type lightly doped areas 20 (as shown in Fig.2);

forming a patterned photo resist layer 22 to cover the conductive layer (gate electrode) 16 in the first region I, and the second region II (as shown in Fig.3);

performing a second implantation process to implant N type dopants into the patterned polysilicon layer 12 to form two N type heavily doped areas 26s and 26d;

removing the patterned photo resist layer 22, and forming another patterned photo resist layer 28 (as shown in Fig.4); and

performing another implantation process to implant P type dopants to from two P type heavily doped areas 32s and 32d in the patterned undoped polysilicon layer 12 in the second region II (as shown in Fig.5).

In US 6,632,709 (see column 9, line 43 to column 10 line 14, and Fig.10(a) to Fig.10(d)), Ayres teaches a method of forming a TFT comprising the steps of:

(d) implanting the semiconductor film, using the mask layer and/or the gate layer as an implantation mask (see col. 1, line 54-55);

(e) etching back the gate layer under the mask layer(see col. 1, line 56); and

a further implantation step after step (f), providing a lower level of doping than step (d) . This produces LDD regions between the source/drain regions formed in step (d) and the gate (see col. 2, line 38-41).

It can be seen that the APA teaches a method of forming

an N type LTPS TFT 34 in which the lightly doped regions 20 are formed **by an implantation process using the gate electrode 16 as a mask**, and the heavily doped regions 26s and 26d are later formed **by forming another patterned photo resist layer 28 as a mask.** Specifically, the lightly doped regions 20 are the heavily doped regions 26s and 26d are formed with different masks **(respectively the gate electrode 16 and the patterned photo resist layer 28)**. In addition, the Ayres' teaching discloses a method of forming a TFT in which the source and drain are formed in step (d), and the LDD regions are then formed after step (e) **(etching back the gate layer as an implantation mask)**. Although Ayres teaches a method of forming the LDD regions in a self-aligned manner as claim1 of the present application does, Ayres fails to teach or suggest performing a trimming process to remove a certain width of the first patterned photo resist layer. The trimming process of the present invention includes performing an ash process, a descum process, and an ultraviolet light beaming process upon the photo resist layer, while the etching back process according to Ayres' teaching is an etching process acting on the gate layer. As well known in the art, an etching process and a trimming process upon the photo resist layer definitely do not belong to the same scope, and thus the applicant contends that the amended claim 1 including "**performing a trimming process to remove a certain width of the first patterned photo resist layer**" should be patentable over the combination of Ayres and the APA.

In addition, claim 4 has been amended to correct a typographical error and claim 6 has been amended in accordance with the amendment of claim 1. No new matter is entered.

Reconsideration of claims 1-2, 6-9, and 12-17 is hereby requested in view of the above argument. Claims 2, 6-9, and 12-17 are dependent on claim 1 and should be allowable if claim 1 is found allowable.

3. Rejection of claims 3-5 under 35 U.S.C. 103(a) as being unpatentable over the Admitted Prior Art (APA) in view of Ayres (US 6,632,709), and further in view of Yamazaki (US 5,210,050):

Reconsideration of claims 3-5 is politely requested in view of the above arguments for claim 1. As claims 3-5 are dependent on claim 1, claims 3-5 should be allowed if claim 1 is found allowable.

4. Rejection of claims 10 and 11 under 35 U.S.C. 103(a) as being unpatentable over the Admitted Prior Art (APA) in view of Ayres (US 6,632,709), and further in view of Liang (US 5,702,988):

Reconsideration of claims 10 and 11 is politely requested in view of the above arguments for claim 1. As claims 10 and 11 are dependent on claim 1, claims 10 and 11 should be allowed if claim 1 is found allowable.

5. New claims 33-49:

Claim 33 claims a method for forming a self-aligned LTPS TFT, which also comprises the limitation of "performing a trimming process to remove a certain width of the first patterned photo resist layer". This limitation finds support in the specification in paragraph [0025] and Fig.8 for instance,

and no new matter is entered. In addition, none of the cited art teaches or suggests the limitations of claim 33, and explanation has already been presented in the argument over rejection of claim 1.

Claims 34-49 are dependent on claim33, and find support in the specification in paragraph [0023] to [0027] and Fig.6-14.

Consideration of new claims 33-49 is respectfully requested.

6. New claims 50-68:

Claim 50 claims a method for forming a self-aligned LTPS TFT, which also comprises the limitation of "performing a trimming process to remove a certain width of the first patterned photo resist layer". This limitation finds support in the specification in paragraph [0025] and Fig.8 for instance, and no new matter is entered. In addition, none of the cited art teaches or suggests the limitations of claim 50, and explanation has already been presented in the argument over rejection of claim 1.

Claims 51-68 are dependent on claim50, and find support in the specification in paragraph [0023] to [0027] and Fig.6-14.

Consideration of new claims 50-68 is respectfully requested.

Sincerely,

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